REMARKS

Claims 1-9, 11-14, and 16-19 are presented for examination. Claims 14 and 16-19 are allowed. Claims 2-9 and 11-13 are found allowable subject to being rewritten in independent form.

Claim 1 has been rejected under 35 U.S.C. 102(b) as being anticipated by Murthy et al.

This rejection is respectfully traversed for the following reasons.

Independent claim 1 recites a multiport data communication system for transferring data packets between ports. The data communication system comprises a plurality of ports for receiving and transmitting the data packets, and a decision making engine responsive to received data packets for directing the received data packets to the ports selected for transmission of the received data packets.

The decision making engine includes:

- a plurality of queuing devices corresponding to the plurality of ports for queuing data blocks representing the data packets received by the corresponding ports,
- logic circuitry responsive to the plurality of queuing devices for processing the data blocks in accordance with a prescribed algorithm to determine destination information,
- a forwarding circuit responsive to the logic circuitry for identifying at least one transmit port, and

- a traffic capture mechanism for enabling one port of said plurality of ports to output data transferred via multiple other selected ports of said plurality of ports.

In response to Applicant's request to point out specifically wherein Murthy et al discloses each element recited in claim 1, the Examiner has taken the position that "memory is reserved or allocated for each port controller for storing received/transmitted packets. This implies that each of the port controllers stores the data packets as it receives the data packets at its port. Herein (sic), port controllers are the queuing devices as claimed by the applicant in claim 1."

The Examiner's assertion is respectfully traversed for the following reasons.

Murthy discloses that each port controller is allocated 32 Kbytes of shared memory 39 for received packets and 64 Kbytes of shared memory for transmitted packets. The shared memory contains a single Packet Buffer Pool 48 composed of multiple packet buffers 48. The reference specifies that each packet buffer is provided for storing an average sized packet (up to 256 octets). When a longer packet must be handled several packet buffers 47 are used (col. 10, lines 55-63). Accordingly, the reference makes it clear that specific packet buffers are not allocated to particular port controllers.

Further, the reference discloses that packets in the shared memory are handled indirectly using a packet descriptor 49. As packets are processed, the packet descriptor 49 may be copied or moved. However, the packet itself is not moved or copied, it is only referred to via the packet pointer 50. (col. 11, lines 3-9).

Hence, the reference specifically indicates that the port controllers do not queue data blocks representing the data packets received by the corresponding ports, as claim 1 requires. Instead, they place received packets into available packet buffers, where the packets remained unmoved until they are forwarded to a required port.

It is noted that one skilled in the art of data communications would realize that the packet buffers of Murthy are not FIFO buffers. Therefore, the port controllers are not able to perform . queuing.

Hence, Murthy does not disclose the claimed plurality of queuing devices corresponding to the plurality of ports for queuing data blocks representing the data packets received by the corresponding ports.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied*, 110 S.Ct. 154 (1989).

As demonstrated above, Murthy does not disclose each element of clam 1. Therefore, the Examiner's conclusion of anticipation is not warranted.

In view of the foregoing, and in summary, claims 1-9, 11-14 and 16-19 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Please recognize our Customer No. 20277

as our correspondence address.

Alexander V. Yampolsky Registration No. 36,324

600 13th Street, N.W.

Washington, DC 20005-3096 Phone: 202.756.8000 JAH/AVY/dlb

Facsimile: 202.756.8087

Date: March 25, 2005